ADN2819/ADN2811—Multirate Limiting Amplifier and Clock and Data Recovery ICs

The proprietary delay and phase-locked loop design of the ADN2819 and ADN2811 provide unprecedented jitter performance for robust high-speed networking designs.

Integrated Limiting Amplifier with Adjustable Slice Level Facilitates Design of High-Performance Fiber Optic Receivers

As the demand for bandwidth grows, Analog Devices continues to provide innovative solutions for fiber optic interface ICs that translate into compelling competitive advantages for our customers.

A prime example of Analog's system knowledge and design expertise working together are the ADN2819 and ADN2811. These highly integrated, low-power devices provide adjustable slice level quantization and clock and data recovery functions with the ADN2819 supporting multirate operation up to 2.7 Gbps, and the ADN2811 supporting 2.5/2.7 Gbps data rates only. Diagnostic capabilities include a signal detector with user-adjustable threshold and 3 dB optical hysteresis to prevent chatter, a loss-of-lock detector, and loop-back mode.

The proprietary delay and phase-locked loop architecture of the ADN2819 and ADN2811 ensure that every SONET/SDH jitter requirement is exceeded over all operating conditions. Low bandwidth jitter transfer simultaneous with high bandwidth jitter tolerance and minimal jitter peaking create an ideal scenario in regenerator applications.

Both the ADN2819 and the ADN2811 are user-friendly and flexible. Native and forward error correction (FEC) digital "wrappers" are supported for all rates without any change of reference clock. An internal or external reference clock (at one of four frequencies) can be used, and a multiplexer is incorporated to allow bypass of the CDR. All of these features reduce time to market, minimize costs, and improve manufacturability.

Analog has more than 10 years of experience designing fiber optic components. Put our expertise to work for you.

Features

ADN2819/ADN2811

- Integrated limiting amplifier with adjustable slice
  - Quantizer sensitivity: 6 mV
  - Adjustable slice level: ±100 mV
- Exceeds all SONET/SDH requirements for jitter transfer, generation, and tolerance
- Internal MUX to bypass CDR
- Low power: 550 mW typical
- One supply: 3.3 V ±10%
- Single reference clock frequency for all rates
- Loss-of-lock indicator
- Small footprint: 48-lead LFCSP package (7 mm × 7 mm overall)

ADN2819

- Multirate (155/166 Mbps, 622/666 Mbps, 1.25/1.34 Gbps, 2.49/2.67 Gbps)

ADN2811

- Dual rate 2.5/2.7 Gbps

Applications

- SONET OC–3/12/48, SDH STM–1/4/16, Gb Ethernet, and all associated FEC rates
- WDM transponders
- SONET/SDH regenerators
- SONET/SDH test equipment
- Backplane applications

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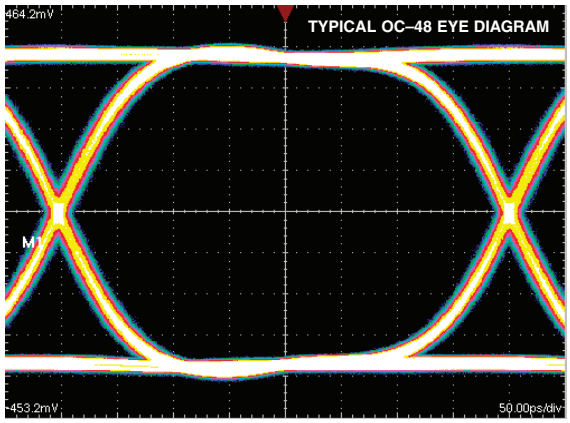
Rate	Typical Jitter Transfer			Typical Jitter Tolerance		
	SONET Spec	ADN2819/ ADN2811	Margin	SONET Spec	ADN2819/ ADN2811	Margin
OC48	2 MHz	666 kHz	3.0	1 MHz	4.8 MHz	4.8
GbE	(1 MHz)	333 kHz	3.0	(500 kHz)	4.8 MHz	9.6
OC12	500 kHz	167 kHz	3.0	250 kHz	4.8 MHz	19.2
OC3	130 kHz	41 kHz	3.2	65 kHz	0.6 MHz	9.2

Exceeds all SONET/SDH jitter requirements for exceptional performance

PRBS23 PATTERN



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